What is claimed is:

1. A semiconductor device, comprising:

a non-volatile memory cell array including a plurality of word lines, a plurality of bit lines intersected with the a plurality of word lines, and a plurality of non-volatile memory cells arranged at respective positions where the a plurality of word lines are intersected with the a plurality of bit lines;

a write buffer for supplying a write signal corresponding to write data;

an input buffer for supplying the write data to the write buffer; and

a write data register connected to the input buffer and holding the write data.

2. A semiconductor device according to claim 1, further comprising:

an address register for holding an address input from external; and

a comparator for comparing an address held in the address register with an input address;

wherein the semiconductor device outputs the write data held in the data register if the comparator indicates that the address held in the address register agrees with the input address.

3. A semiconductor device according to claim 2

wherein the comparator makes a comparison at subsequent read access after write is done to the non-volatile memory cell array.

4. A semiconductor device according to claim 2 wherein if the comparator indicates that the address held in the address register agrees with the input address, the semiconductor device performs no read operation from the non-volatile memory cell array.

5. A semiconductor device according to claim 4, further comprising:

a sense amplifier block which supplies a read voltage to a selected bit line of the a plurality of bit lines in the read operation;

wherein the sense amplifier block does not supply the read voltage if the comparator indicates that the address held in the address register agrees with the input address.

6. A semiconductor device according to claim 1, further comprising an address transition detector which detects an address transition.

7. A semiconductor device according to claim 1 wherein the a plurality of non-volatile memory cells each have a phase change resistor.

8. A semiconductor device, comprising:

a memory cell array including a plurality of word lines, a plurality of bit lines which are intersected with

the a plurality of word lines, and a plurality of memory cells which are arranged at respective positions where the a plurality of word lines are intersected with the a plurality of bit lines;

a write buffer for supplying a write signal corresponding to write data;

an input buffer for supplying the write data to the write buffer;

a write data register connected to the input buffer and holding the write data; and

a flag register for holding a flag,

wherein the flag indicates whether the write data held in the write data register is valid.

9. A semiconductor device according to claim 8 wherein the flag register is set by a write operation.

10. A semiconductor device according to claim 9 wherein the flag register is reset when the semiconductor device is powered on.

11. A semiconductor device according to claim 9 wherein the flag register is reset when a desirable period of time has lapsed after the write operation.

12. A semiconductor device according to claim 8, further comprising:

an address register for holding an address input from external; and

a comparator for comparing an address held in the

address register with the next input address;

wherein the comparator performs the comparing operation if the flag indicates the write data is valid and does not perform the comparing operation if the flag indicates the write data is invalid.

13. A semiconductor device according to claim 8, further comprising an address transition detector which detects an address transition.

14. A semiconductor device according to claim 8 wherein each of the a plurality of memory cells is a non-volatile memory cell.

15. A semiconductor device according to Claim 8 wherein each of the a plurality of memory cells has a phase change resistor.

16. A semiconductor device, comprising:

a non-volatile memory cell array including a plurality of word lines, a plurality of bit lines intersected with the a plurality of word lines, and a plurality of non-volatile memory cells arranged at respective positions where the a plurality of word lines are intersected with the a plurality of bit lines; and

a write data register for holding write data which is written into the a plurality of non-volatile memory cells;

wherein if write access is followed by read access, a first address for the write access is compared with a

second address for the read access and the write data held in the write data register is read out if the first address agrees with the second address.

17. A semiconductor device according to claim 16 wherein the comparing operation is performed if the write data is valid and not performed if the write data is invalid.

18. A semiconductor device according to claim 17, further comprising a flag which indicates the write data is valid or invalid;

wherein the flag indicates the write data is valid when the write access occurs and the write date is invalid after a predeterminant period of time has lapsed.

19. A semiconductor device according to claim 16 wherein a read voltage is supplied to a selected bit line of the a plurality of bit lines when data is read out from the non-volatile memory cell array whereas the read voltage is not supplied when the data held in the write data register is read out.

20. A semiconductor device according to Claim 16 wherein each of the a plurality of non-volatile memory cells has a phase change memory.